Date: **18/03/2026** **CS29204**: Switching Circuits Laboratory

# Assignment 7

Design of shift registers


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## Part (a)

### Aim

To design a 4-bit bidirectional shift register using D flip-flops, and configure it in right-shift mode, apply the pattern 00110011..., and verify the output.

### Apparatus

- Breadboard
- IC 7474 × 2 (Dual D Flip-flop)
- IC 74157 × 1 (Quad 2-to-1 MUX)
- Wires, wire cutter, tweezers

### Theory

A bidirectional shift register is a type of register which can do both left and right shifts per clock pulse, based on an $L/R'$ input. It can be designed using D flip-flops, and 2x1 MUXes can be used to select the mode of operation.

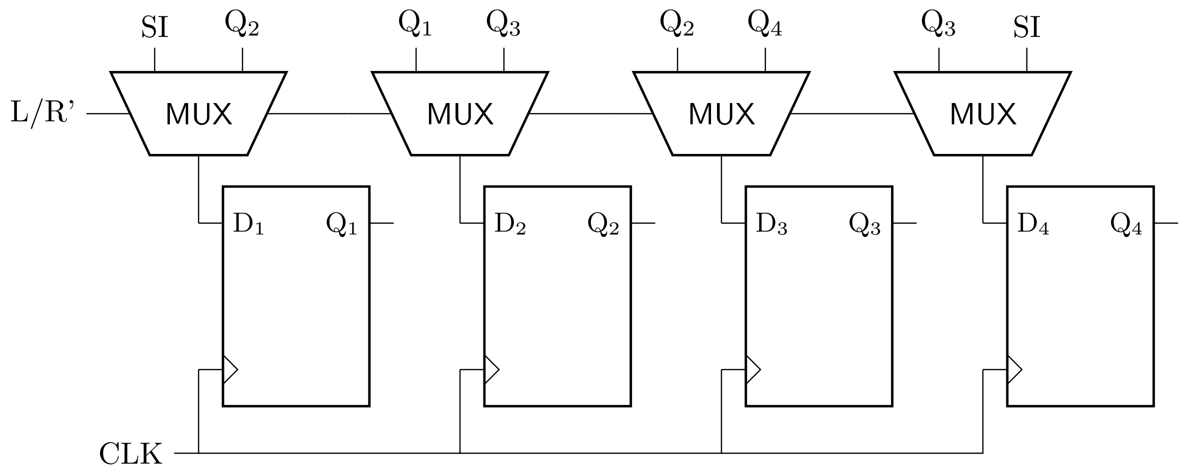


**Figure 1:** A 4-bit bidirectional shift register

If $L/R' = 0$, then the circuit is configured in right-shift mode, so the input at SI (Serial Input) is shifted into $Q_1$, $Q_2$, $Q_3$, and $Q_4$ sequentially, at each clock pulse.

Similarly, if $L/R' = 1$, then the circuit is configured in left-shift mode, so the input at SI (Serial Input) is shifted into $Q_4$, $Q_3$, $Q_2$, and $Q_1$ at each clock pulse.

Since we need to configure the circuit in right-shift mode, we will set $L/R' = 0$.

In the Serial Input, we need to give the input pattern 00110011... in synchronism with the clock. Based on this input, the circuit will shift the data into the flip-flops sequentially.

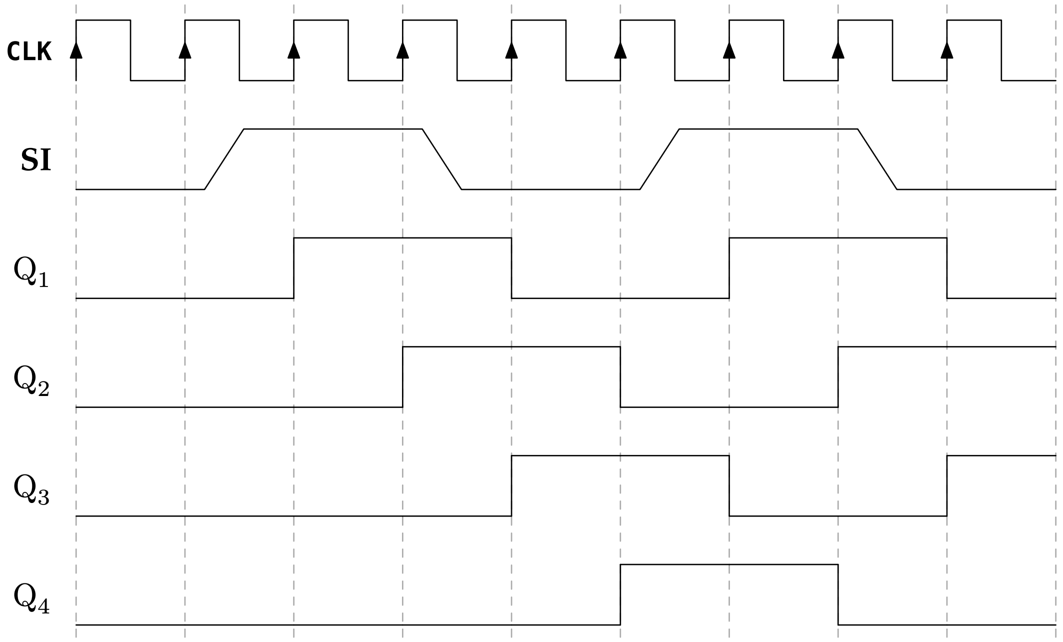


**Figure 2:** Timing diagram of the serial input and the shift register

So what we will observe, is that the values of $Q_1, Q_2, Q_3, Q_4$ will cycle through $\{0000, 1000, 1100, 0110, 0011, 1001, 1100, ...\}$.

## Circuit Diagram

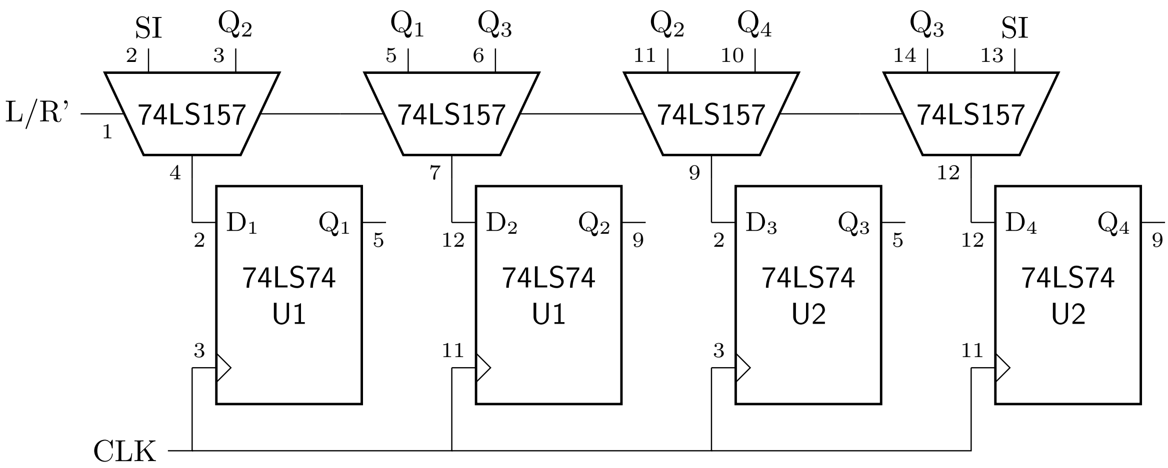


**Figure 3:** Circuit diagram of a 4-bit bidirectional shift register

## Procedure

1. Realise a 4-bit bidirectional shift register, as shown in Figure 3.
2. Configure the circuit in right-shift mode, by setting $L/R' = 0$.
3. Apply a slow clock signal to the clock input. Connect the inputs and outputs.
3. Apply the input pattern 00110011... to the serial input, and observe the output.

## Observations

The pattern 1100 shifts right continuously at each clock pulse.

# Part (b)

## Aim

To modify the bidirectional shift register to implement

(i) A 4-bit ring counter.

(ii) A 4-bit linear feedback shift register, which realises the characteristic polynomials $f(x) = x^4 + x + 1$ and $f(x) = x^4 + x^3 + x + 1$.

## Apparatus

- Breadboard
- IC 7486 × 1 (Quad Exclusive OR)
- Wires, wire cutter, tweezers

## Theory

A **ring counter** is a circuit obtained by connecting the Q output of the last flip-flop in a shift register to the D input of the first flip-flop (Serial In).

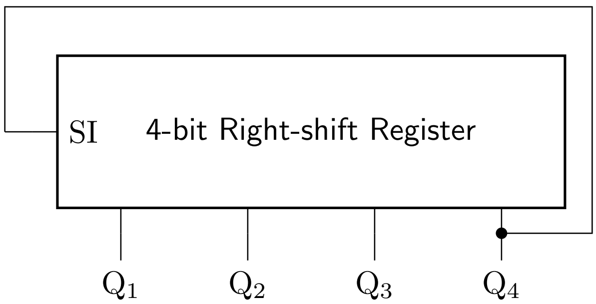


**Figure 4:** Circuit diagram of a ring counter

We can initialise the register with the pattern 1000, and then it will keep shifting the data right, thus counting in the order $\{1000, 0100, 0010, 0001, ...\}$.

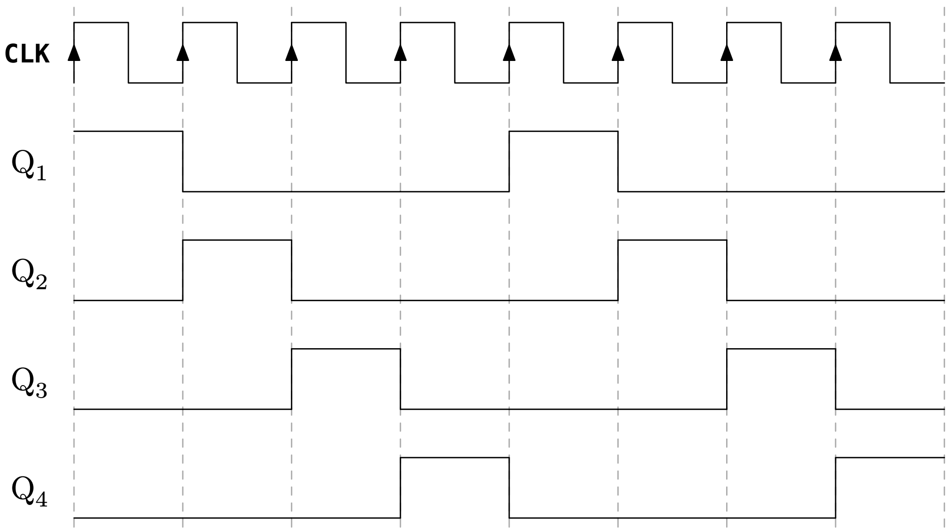


**Figure 5:** Timing diagram of the ring counter

Thus, we get a multi-phase clock, or a sequence of synchronising (non-overlapping) pulses.

A **linear feedback shift register** (LFSR) is serial-in serial out (SISO) right shift register, where the serial input is generated as a linear function (XOR) of some of the flip-flop outputs.

The characteristic polynomial of a LFSR encodes which flip-flop outputs are used in the feedback connection.

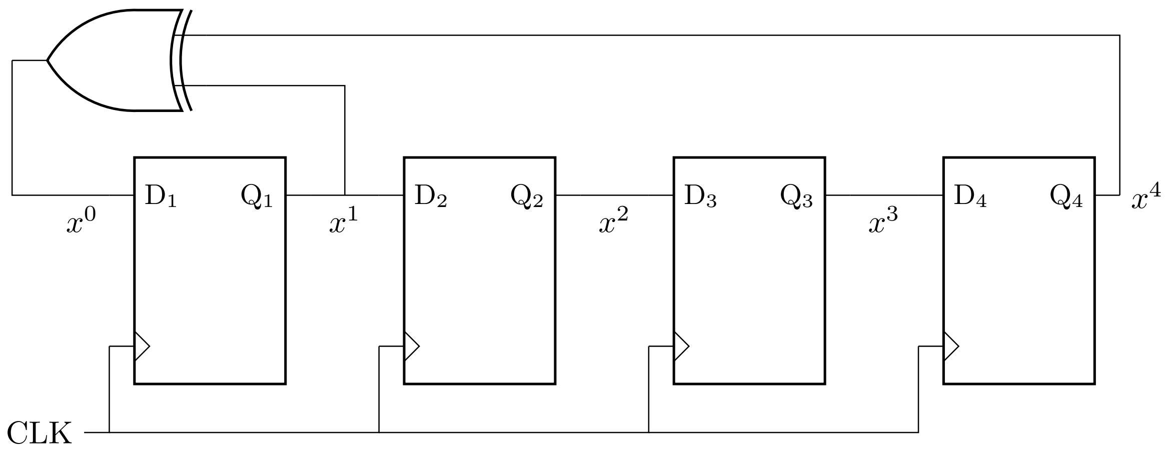


**Figure 6:** A Linear Feedback Shift Register with characteristic polynomial $f(x) = x^4 + x + 1$

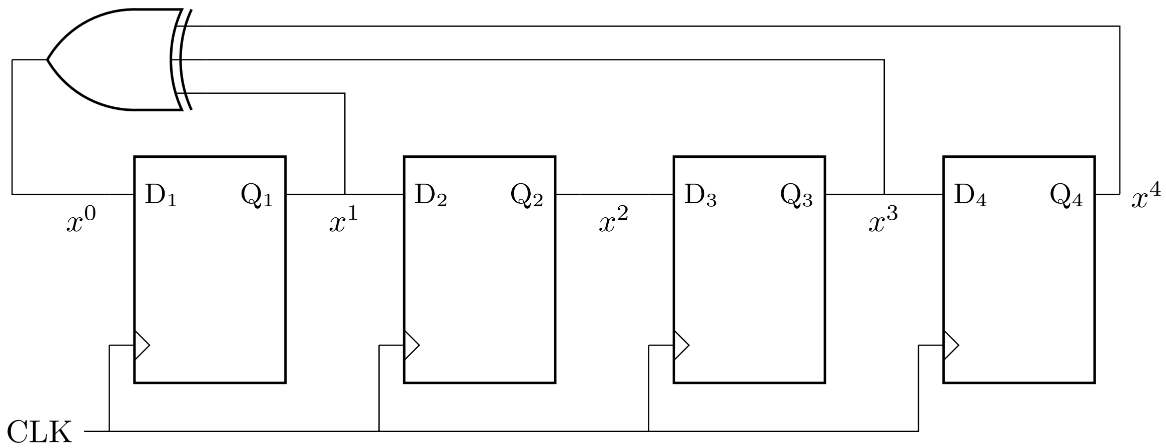


**Figure 7:** A Linear Feedback Shift Register with characteristic polynomial $f(x) = x^4 + x^3 + x + 1$

We can initialise the register with 1000 (using asynchronous preset/clear), and then the LFSR cycles through a sequence of values, which is characterised by the characteristic polynomial.

| $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ |
|---|---|---|---|
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 |

**Table 1:** Sequence of values for a LFSR with characteristic polynomial $f(x) = x^4 + x + 1$

| $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ |
|---|---|---|---|
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 |

**Table 2:** Sequence of values for a LFSR with characteristic polynomial $f(x) = x^4 + x^3 + x + 1$

## Circuit Diagram

In the following diagrams, only pin numbers for additional connections required over Figure 3 are depicted.

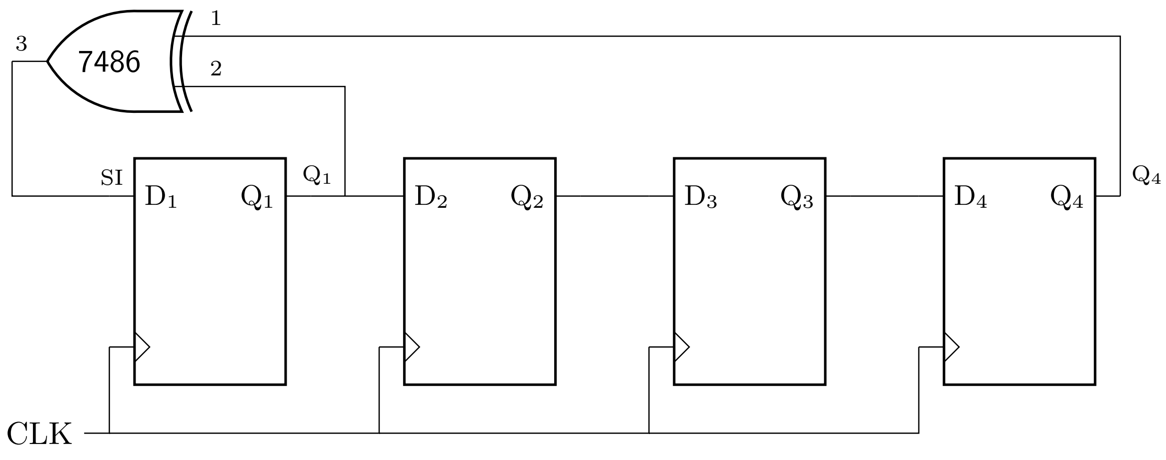


**Figure 8:** Circuit diagram of a 4-bit LFSR with characteristic polynomial $f(x) = x^4 + x + 1$

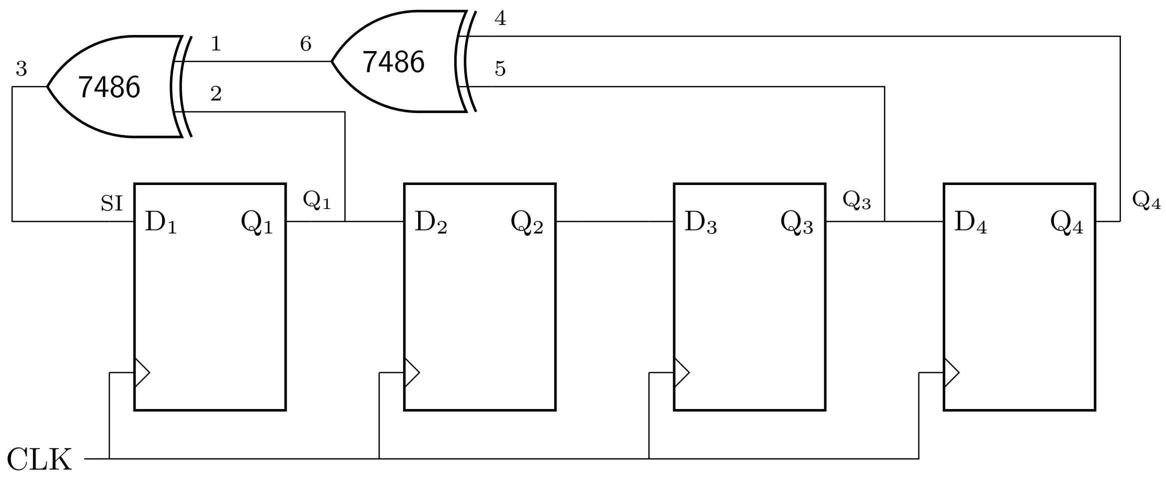


**Figure 9:** Circuit diagram of a 4-bit LFSR with characteristic polynomial $f(x) = x^4 + x^3 + x + 1$

## Procedure

Ring Counter:

1. Connect the $Q_4$ output of the last flip-flop back to the Serial Input (SI) of the first flip-flop, forming a ring.
2. Initialise the register to the pattern 1000 using the asynchronous preset/clear inputs.
3. Apply a clock signal of sufficiently high frequency.
4. Observe the output waveforms on the oscilloscope.

Linear Feedback Shift Register:

1. Connect an XOR gate with inputs $Q_1$ and $Q_4$ (corresponding to the characteristic polynomial $f(x) = x^4 + x + 1$) to the SI input.
2. Initialise the register to 1000 using the asynchronous preset/clear inputs.
3. Apply a slow clock signal and record the 4-bit pattern at the outputs.
4. Repeat the procedure with the feedback taken as $Q_1 \oplus Q_3 \oplus Q_4$ for the characteristic polynomial $f(x) = x^4 + x^3 + x + 1$.

## Observations

1. The ring counter correctly counts in the order $\{1000, 0100, 0010, 0001, 1000, ...\}$. The output in the oscilloscope resembles Figure 5.
2. LFSR with characteristic polynomial $f(x) = x^4 + x + 1$ loops through the 15 states:

$$\begin{gathered} 1000 \to 1100 \to 1110 \to 1111 \to 0111 \to \\ 1011 \to 0101 \to 1010 \to 1101 \to 0110 \to \\ 0011 \to 1001 \to 0100 \to 0010 \to 0001 \end{gathered}$$

3. LFSR with characteristic polynomial $f(x) = x^4 + x^3 + x + 1$ loops through the 6 states:

$$1000 \to 1100 \to 1110 \to 0111 \to 0011 \to 0001$$