Date: **11/03/2026** **CS29204**: Switching Circuits Laboratory

Assignment 6

Design of flip-flops

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Part (a)

Aim

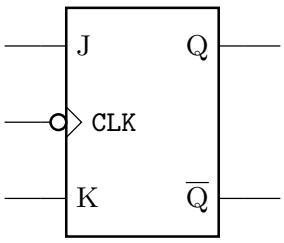
To design a J-K master slave flip-flop using NAND gates and verify its functionality, and to convert it into a T flip flop and demonstrate that it divides the frequency of an incoming rectangular waveform by 2.

Apparatus

- Breadboard
- IC 7400 × 2 (TTL Quad 2-input NAND gate)
- IC 7410 × 1 (TTL Triple 3-input NAND gate)
- Digital Storage Oscilloscope
- Wires, wire cutter, tweezers

Theory

A J-K flip-flop is a type of flip flop which has two inputs, J and K, and two outputs, Q and Q'. It is clock edge-triggered, and at an active clock edge, based on its J and K inputs, it correspondingly sets the output Q according to the state table shown below.



CLK	J	K	Q_{n+1}	$\overline{Q_{n+1}}$
0/1	X	X	Q_n	$\overline{Q_n}$
↓	0	0	Q_n	$\overline{Q_n}$
↓	0	1	0	1
↓	1	0	1	0
↓	1	1	$\overline{Q_n}$	Q_n

Figure 1: A negative edge triggered J-K flip-flop and its state table

To design a J-K master slave flip-flop, we essentially need two cross-coupled latches, one acting as the master and the other as the slave. The clock signal is the enable signal for the master latch, and it is inverted to be the enable signal for the slave latch. The slave latch's output feeds back into the master latch's input, for the functioning of the J-K flip-flop.

To verify the functionality of the J-K master slave flip-flop, we can apply different combinations of J and K inputs and verify that the output follows the expected state transitions.

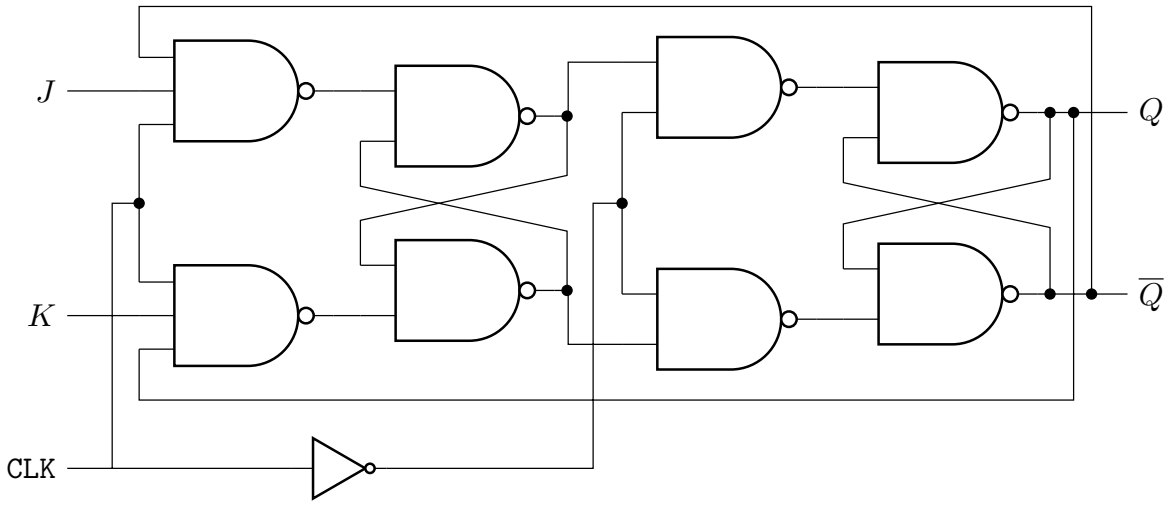
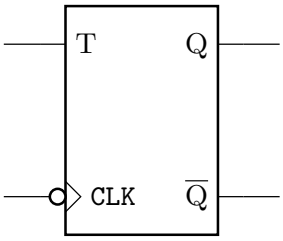


Figure 2: Circuit diagram of a J-K master slave flip-flop

A T flip-flop is a type of flip-flop which only has a single input (T), and when T = 1, at the active edge of the clock signal, the flip-flop toggles its state.



CLK	T	Q_{n+1}	$\overline{Q_{n+1}}$
0/1	X	Q_n	$\overline{Q_n}$
↓	0	Q_n	$\overline{Q_n}$
↓	1	$\overline{Q_n}$	Q_n

Figure 3: A negative edge triggered T flip-flop and its state table

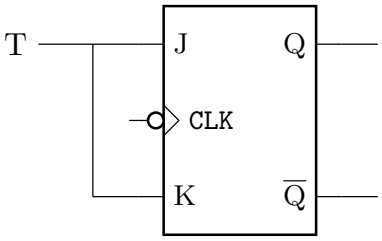


Figure 4: Implementing a T flip-flop using a J-K flip-flop

We can implement a T flip-flop using a J-K flip-flop by connecting the J and K inputs together, as the T input.

Once we have a T flip-flop, if we set T = 1 (constant), it will toggle its state Q at each clock edge, thus the output signal will be a rectangular waveform, with double the time period of the clock signal.

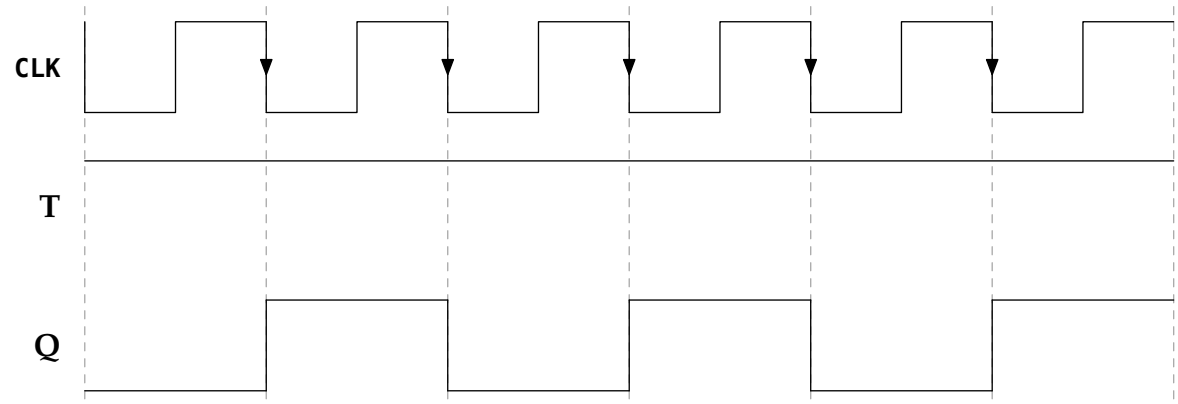


Figure 5: Generating a rectangular waveform with a T flip-flop

Circuit Diagram

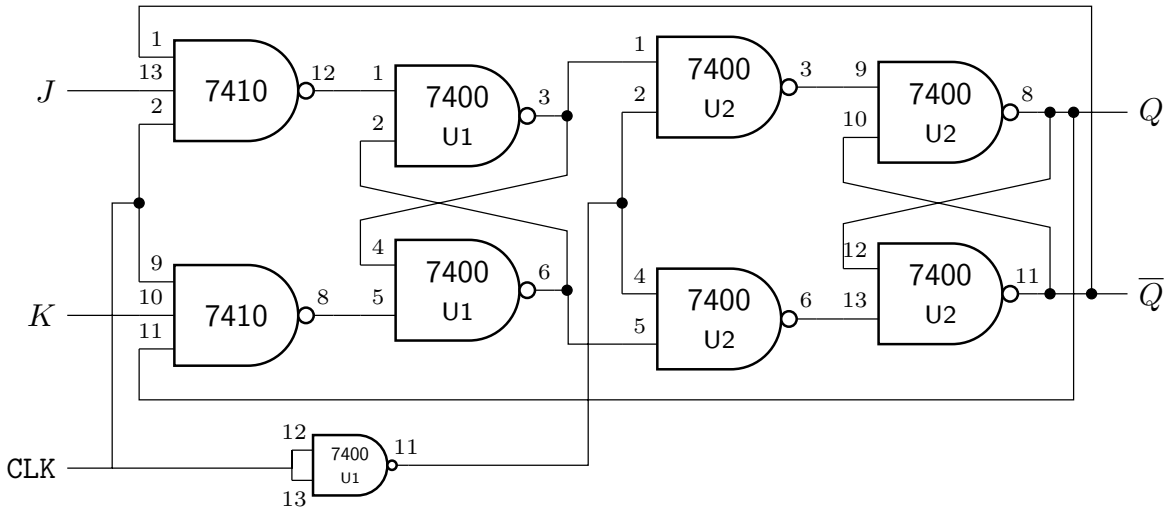


Figure 6: Circuit diagram of a J-K flip-flop in master-slave configuration

Procedure

1. Using NAND gates, realise a master slave J-K flip-flop, as shown in Figure 6.
2. Connect the inputs to the circuit, and verify the working of the J-K flip-flop under different input combinations of J and K. Check if the output correctly transitions as per the state table.
3. Tie the J and K inputs together, thus realising a T flip-flop.
4. Connect the T input to constant high (1), and input a periodic waveform at the clock input. Observe the output waveform on the oscilloscope, and measure its frequency.

Observations

- Frequency of clock signal: 3.3 kHz
- Frequency of output waveform: 1.65 kHz

Results

1. The J-K flip-flop works correctly; the output changes correctly according to the state table at the active clock edge.
2. The T flip-flop generates a rectangular waveform at the output, with the frequency half of the clock frequency.

Part (b)

Aim

To design a J-K latch using NAND gates, and connect an edge detection circuit block to its enable input, and verify its operation.

Apparatus

- Breadboard
- IC 7400 × 1 (TTL Quad 2-input NAND gate)
- IC 7410 × 1 (TTL Triple 3-input NAND gate)
- IC 7404 × 1 (TTL Hex Inverter)
- Wires, wire cutter, tweezers

Theory

We can create a J-K latch using NAND gates by taking a gated S-R latch, and adding feedback from the outputs (Q and Q′) to the input NAND gates.

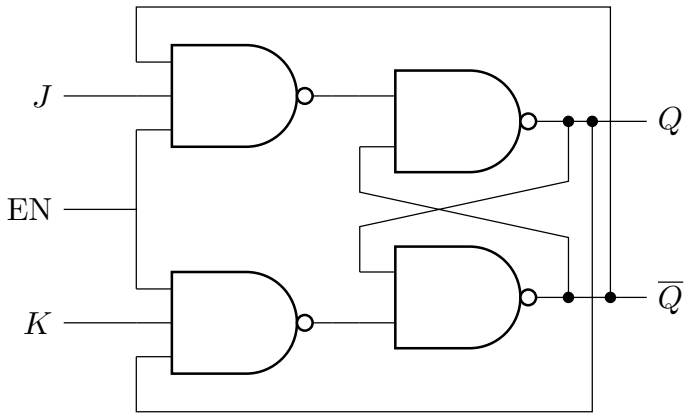


Figure 7: Circuit diagram for a J-K latch with enable input

To convert this into a flip-flop, we need to first construct an edge detection circuit block, which will detect a rising edge of the clock signal, and generate a narrow pulse on every rising edge. If we apply this new signal to the enable input of the J-K latch, the circuit will behave as a flip-flop, which changes state according to the inputs J and K on every rising edge of the clock.

We can implement edge detection by sending the clock signal into two inputs of a NAND gate, one connected directly, and the other through an odd number of inverters. Due to the propagation delay of the inverters, the output will have a short pulse on every rising edge of the clock.

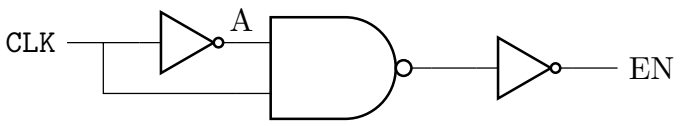


Figure 8: Circuit diagram for an edge detection circuit

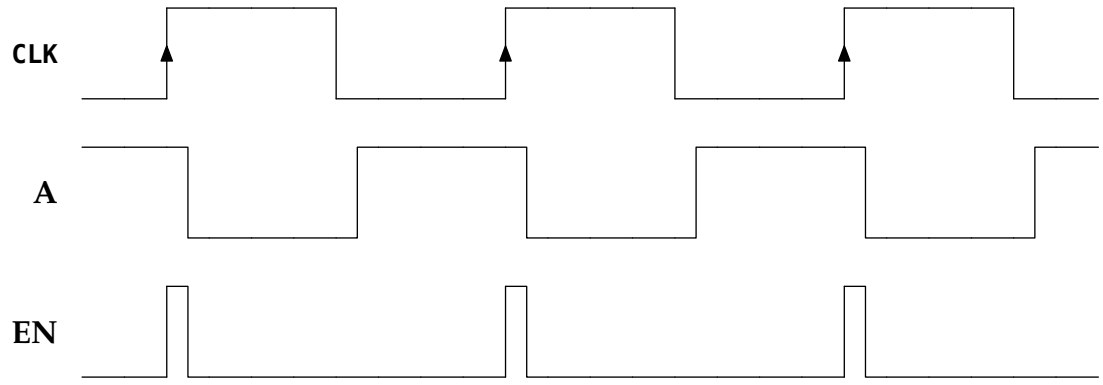


Figure 9: Output of the edge detection circuit

We can connect this edge detection circuit block to the enable input of the J-K latch to create a flip-flop. To verify the working of the J-K flip-flop, we can apply different input combinations to the J and K inputs and verify that the output Q transitions correctly, according to the state table.

Circuit Diagram

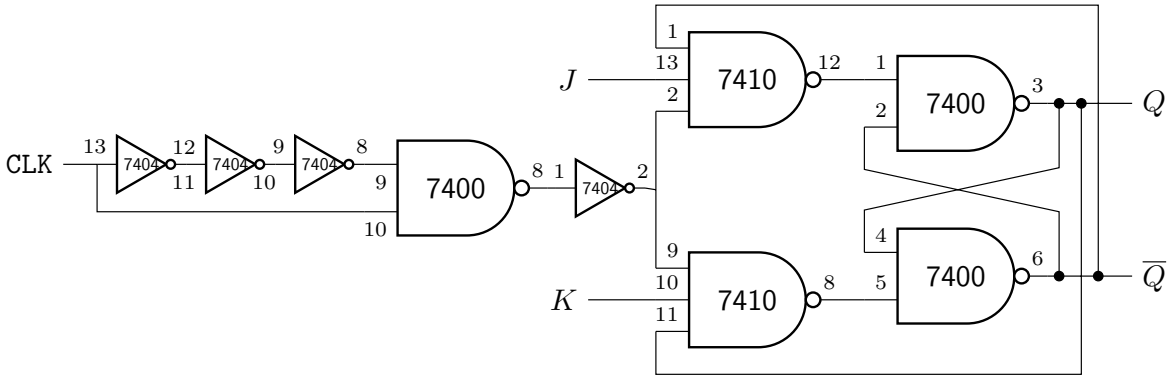


Figure 10: Circuit diagram for a J-K flip-flop with edge detection

Procedure

1. Using NAND gates, implement a J-K latch, as shown in Figure 7.
2. Add an edge detection circuit block to the clock input of the J-K latch.
3. Verify the working of the J-K flip-flop by applying different input combinations to the J and K inputs. Check if the output Q transitions correctly according to the state table.

Results

The J-K flip-flop works as expected. The edge-detection circuit block operations work correctly.

Discussion

When the edge detection circuit block was realised with a single inverter, the narrow pulse that was generated at the enable input was not large enough to trigger the J-K latch. Changing the circuit design to use 3 inverters instead increased the pulse's amplitude, allowing it to trigger the latch correctly.