Date: **28/01/2026** **CS29204**: Switching Circuits Laboratory

# Assignment 3

Design of combinational circuit, with clock generator and binary counter

**Group 36**
Dipam Sen (24CS10059)
Mitali Laddha (24CS10111)

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## Part (a)

### Aim

To design a combinational circuit $C$ that converts a 4-bit binary number $B = (b_3, b_2, b_1, b_0)$ into a two digit BCD number $(T, U)$ (using NAND, NOR and NOT gates), and display them on 7-segment display units.

### Apparatus

- Breadboard
- IC 7400 × 3 (TTL IC Quad NAND Gate)
- IC 7404 × 1 (TTL IC Hex Inverter)
- IC 7447 × 2 (BCD to Seven Segment Decoder)
- Seven Segment Display Unit (Common Anode) × 2
- Wires, wire cutter, tweezers, resistors

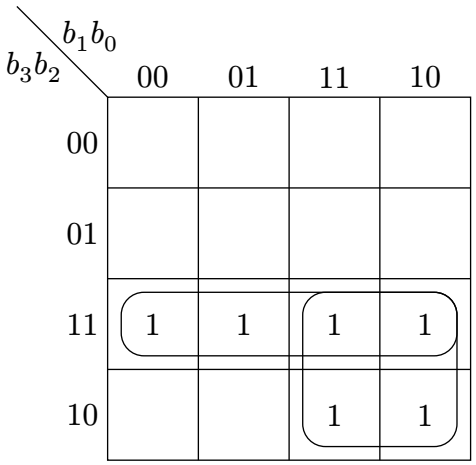
### Theory

First, we need to draw the truth table for the conversion of the 4-bit input to BCD digits.

| $B$ | $b_3$ | $b_2$ | $b_1$ | $b_0$ | $T$ | $U$ | $t_3$ | $t_2$ | $t_1$ | $t_0$ | $u_3$ | $u_2$ | $u_1$ | $u_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 | 0 | 2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 | 0 | 3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 | 0 | 4 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 | 0 | 5 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 | 0 | 6 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 | 0 | 7 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 | 0 | 8 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 | 9 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 11 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 12 | 1 | 1 | 0 | 0 | 1 | 2 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 13 | 1 | 1 | 0 | 1 | 1 | 3 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 14 | 1 | 1 | 1 | 0 | 1 | 4 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 15 | 1 | 1 | 1 | 1 | 1 | 5 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |

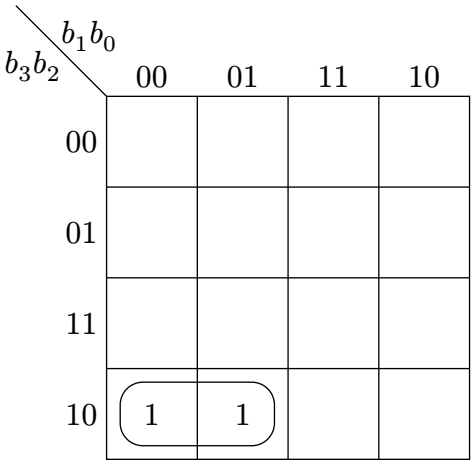
**Table 1:** Truth table for converting a 4-bit binary number into 2 BCD digits

To realise these functions as circuits, we need their minimal switching expressions, which we can get by using Karnaugh maps. (The functions $t_3$, $t_2$, $t_1$ are constant 0.)



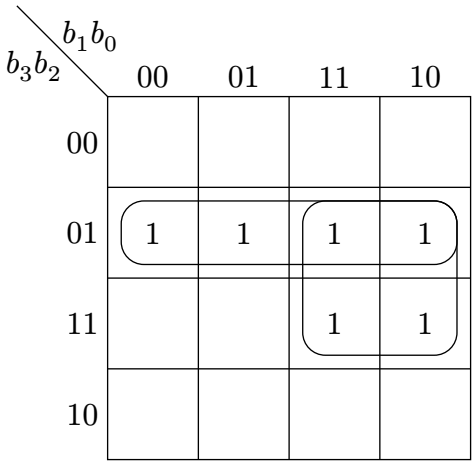

$t_0 = \Sigma(10, 11, 12, 13, 14, 15)$

$t_0 = b_3b_2 + b_3b_1$



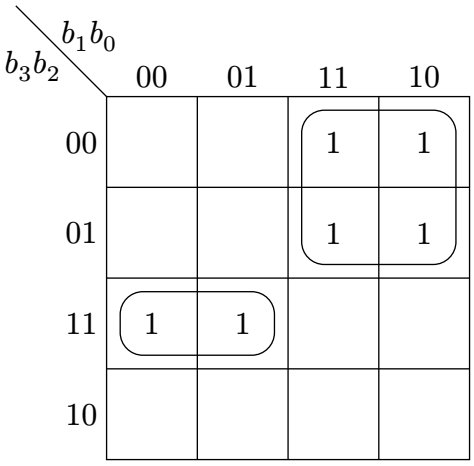

$u_3 = \Sigma(8, 9)$

$u_3 = b_3b_2'b_1'$



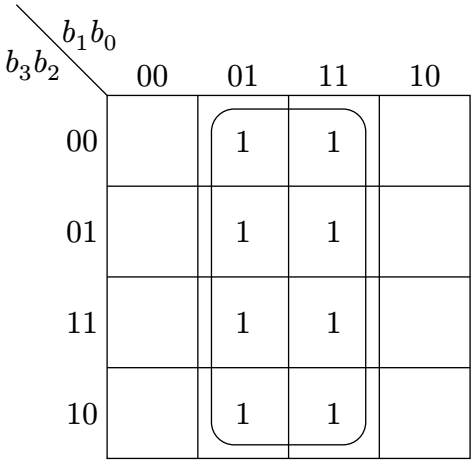

$u_2 = \Sigma(4, 5, 6, 7, 14, 15)$

$u_2 = b_3'b_2 + b_2b_1$




$u_1 = \Sigma(2, 3, 6, 7, 12, 13)$

$u_1 = b_3'b_1 + b_3b_2b_1'$




$u_0 = \Sigma(1, 3, 5, 7, 9, 11, 13, 15)$

$u_0 = b_0$

**Figure 1:** Karnaugh maps for functions $t_3$, $u_3$, $u_2$, $u_1$ and $u_0$ and their minimal SoP expressions.

Thus we have found the following expressions for the 8 switching functions in terms of the 4 inputs $b_3$, $b_2$, $b_1$ and $b_0$:

$$t_3 = 0$$
$$t_2 = 0$$
$$t_1 = 0$$
$$t_0 = b_3b_2 + b_3b_1$$

$$u_3 = b_3b_2'b_1'$$
$$u_2 = b_3'b_2 + b_2b_1$$
$$u_1 = b_3'b_1 + b_3b_2b_1'$$
$$u_0 = b_0$$

Since these are minimal sum-of-product expressions, we can implement them using only NAND gates and NOT gates.

The 8-bit output needs to be displayed on two 7-segment display units. For this we use IC 7447 (BCD to 7 Segment Decoder) along with two common anode display units.

## Procedure

1. Draw the truth table for the given functions.
2. For each output, obtain a simplified logic expression by using Karnaugh maps.
3. Draw a circuit diagram for the gate level realisation of the logic expressions, only using NAND, NOR and NOT gates.
4. Connect the circuit on the breadboard.
5. Connect the ouputs to the BCD to 7 segment decoders and then to the display units.
6. For each input combination (0-15), verify that the displays correctly show the number's tens and units place.

## Circuit Diagrams

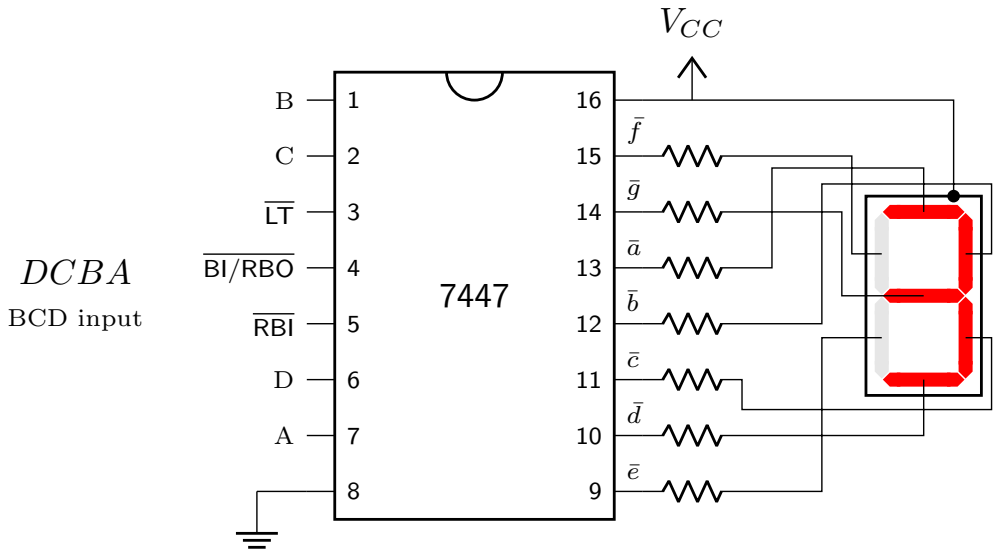



**Figure 2:** Connection diagram for displaying a BCD digit on a 7 Segment Display

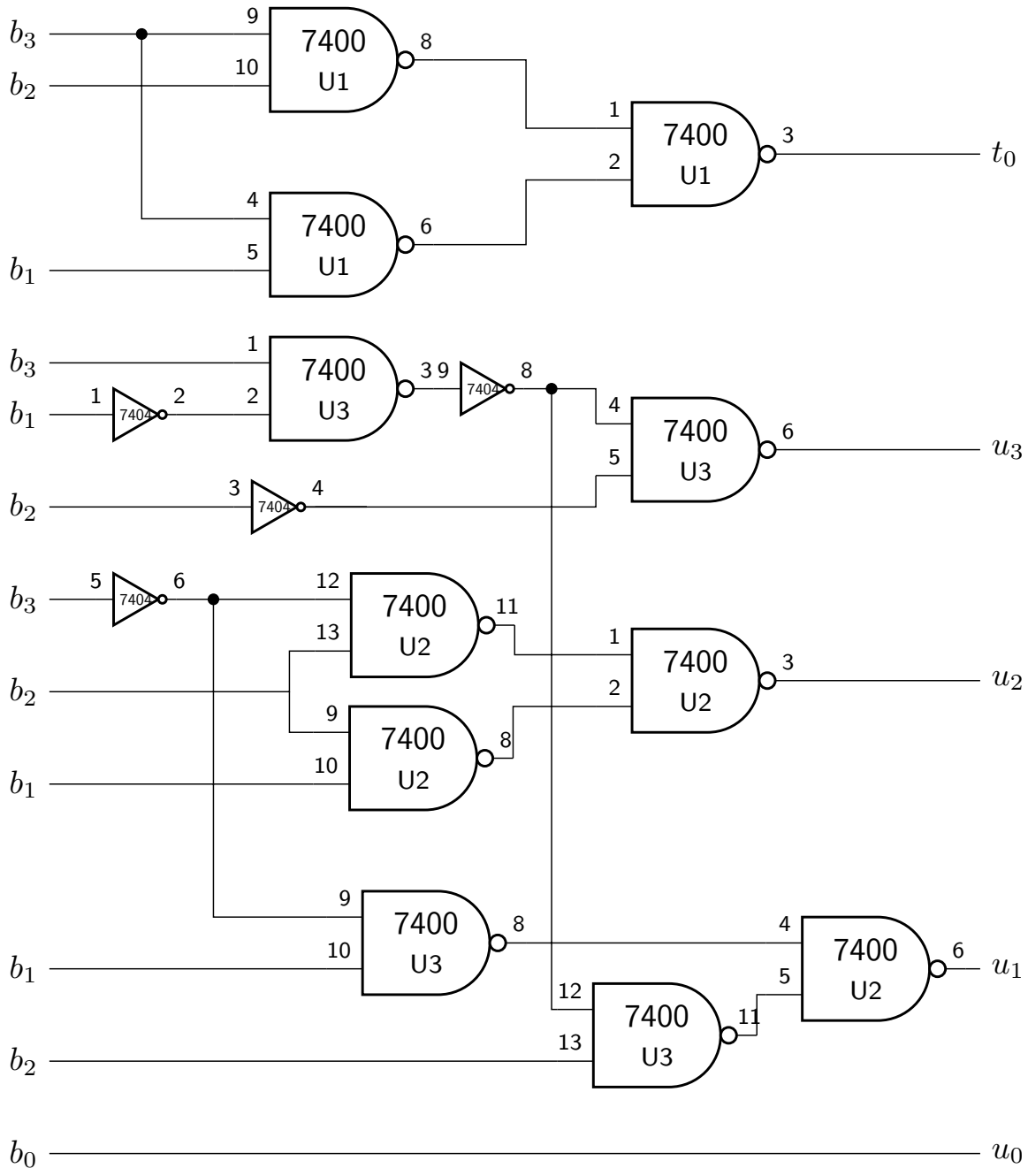



**Figure 3:** Circuit diagram for $C$

## Result

The circuit correctly converts the 4-bit number into 2 BCD digits and displays them on the seven segment displays.

# Part (b)

## Aim

To design an astable multivibrator $M$ using the 555 timer IC to generate a rectangular pulse train of (i) 50 kHz, 90% duty cycle, (ii) 2 Hz, 75% duty cycle.

## Apparatus

- Breadboard
- IC 555 (Timer)
- Resistors, Capacitors
- Digital Storage Oscilloscope
- Wires, wire cutter, tweezers

## Theory

The 555 Timer is a classic IC used for a variety of purposes, including timer, delay and pulse generation. When operated in an **astable** (free running) mode, it can be used as a clock (periodic timer) which has numerous uses. This is referred to as an **astable multivibrator**. The output signal from this is a square wave pulse, which can be used as a clock signal.

Internally, the 555 timer uses a voltage divider, which two comparators use to toggle an internal flip-flop. As the external capacitor charges through the series combination of $R_1$ and $R_2$, the output remains high until the voltage reaches a threshold, at which point the flip-flop resets and the output goes low. This activates an internal discharge transistor that allows the capacitor to discharge through $R_2$; once the voltage drops below a threshold, the flip-flop sets again, cutting off the discharge path and restarting the cycle to produce a continuous rectangular pulse.

The shape of the output signal can be controlled by the external resistors and capacitors connected in the circuit.

Let $t_1$ denote the time during which the capacitor charges, and $t_2$ be the time during which the capacitor discharges. Then, we have the following relations.

$$t_1 = 0.693(R_1 + R_2)C$$
$$t_2 = 0.693R_2C$$
$$T = t_1 + t_2 = 0.693(R_1 + 2R_2)C$$

$$\text{Frequency } f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)C}$$

$$\text{Duty Cycle} = \frac{t_1}{T} \times 100\%$$

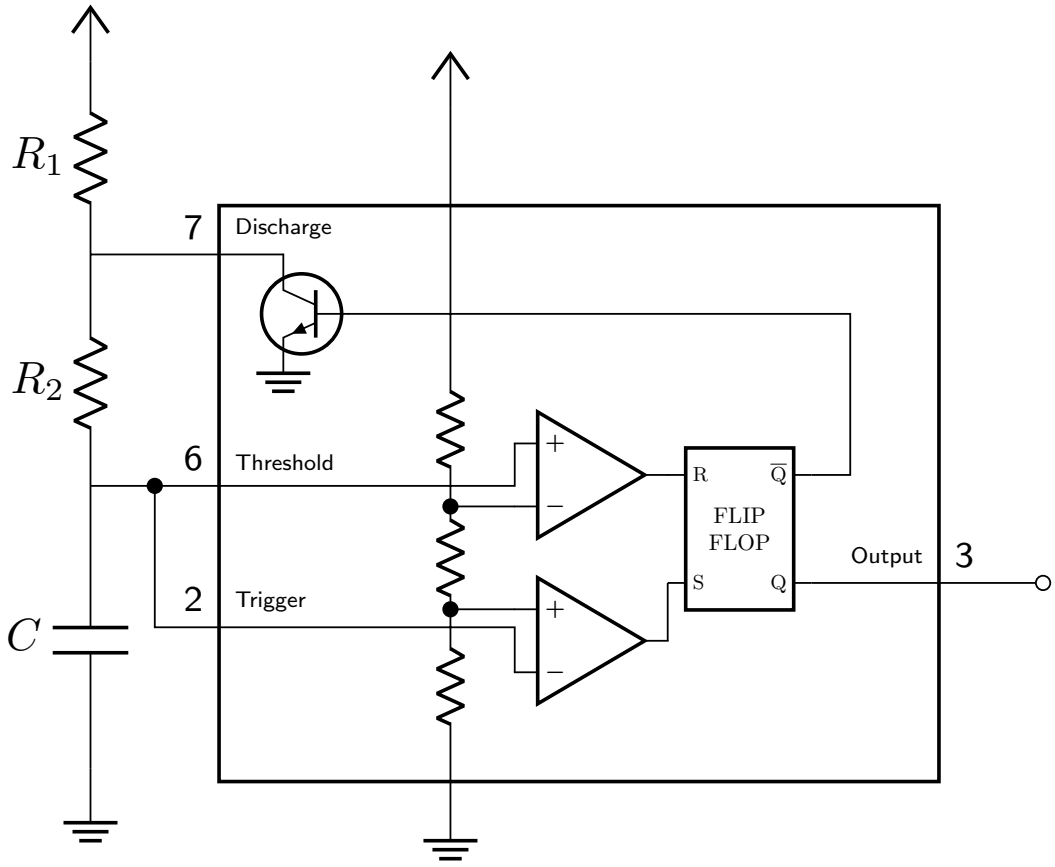



**Figure 4:** Circuit diagram for an astable multivibrator using the 555 timer

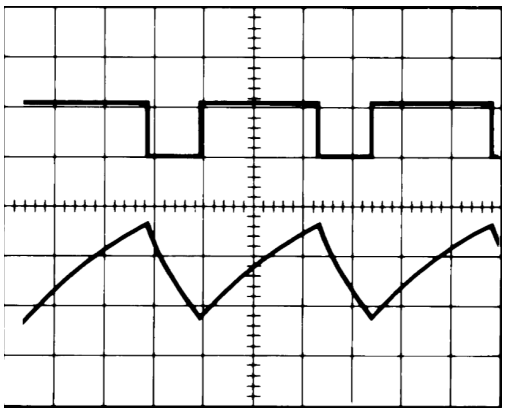


**Figure 5:** Output signal (top) and voltage across the capacitor (bottom)

## Calculations

(i) $f = 50\,\text{kHz}, \text{DC} = 90\%$

Take $C = 10\,\text{pF}$.

$$T = \frac{1}{f} = \frac{1}{50\,\text{kHz}} = 2 \times 10^{-5}\,\text{s}$$

$$t_1 = 0.9 \times T = 1.8 \times 10^{-5}\,\text{s}$$
$$t_2 = 0.1 \times T = 2 \times 10^{-6}\,\text{s}$$

$$t_1 = 0.693(R_1 + R_2)C$$
$$\Rightarrow R_1 + R_2 = \frac{t_1}{0.693C} = \frac{1.8 \times 10^{-5}\,\text{s}}{0.693 \times 10\,\text{pF}} = 2597.4\,\Omega$$

$$t_2 = 0.693R_2C$$
$$\Rightarrow R_2 = \frac{t_2}{0.693C} = \frac{2 \times 10^{-6}\,\text{s}}{0.693 \times 10\,\text{pF}} = 288.6\,\Omega$$
$$\Rightarrow R_1 = 2308.8\,\Omega$$

We take $R_1 = 2\,\text{k}\Omega$, $R_2 = 270\,\Omega$.

(ii) $f = 2\,\text{Hz}, \text{DC} = 75\%$

Take $C = 0.1\,\mu\text{F}$.

$$T = \frac{1}{f} = \frac{1}{2\,\text{Hz}} = 0.5\,\text{s}$$
$$t_1 = 0.75 \times T = 0.375\,\text{s}$$
$$t_2 = 0.25 \times T = 0.125\,\text{s}$$

$$R_1 + R_2 = \frac{t_1}{0.693C} = \frac{0.375\,\text{s}}{0.693 \times 0.1\,\mu\text{F}} = 5.4\,\text{M}\Omega$$
$$R_2 = \frac{t_2}{0.693C} = \frac{0.125\,\text{s}}{0.693 \times 0.1\,\mu\text{F}} = 1.8\,\text{M}\Omega$$
$$\Rightarrow R_1 = 3.6\,\text{M}\Omega$$

We take $R_1 = 3.6\,\text{M}\Omega$, $R_2 = 1.8\,\text{M}\Omega$.

## Procedure

1. Connect the 555 timer to the breadboard.
2. Connect the external resistors and capacitors (as calculated) to the breadboard, and the remaining connections for the astable multivibrator accordingly.
3. Display the output signal on the oscilloscope. Verify the frequency of the output signal.

## Observations

(i) The frequency of the output signal is 50.5 kHz.
(ii) The frequency of the output signal is 2.5 Hz.

## Result

The astable multivibrator correctly generates a square wave pulse train of the required frequency and duty cycle.

# Part (c)

## Aim

To feed the clock signal from $M$ (part (b)) to a 4-bit binary counter, and feed its output to circuit $C$ (part (a)) to display the number on the 7-segment display.

## Apparatus

- Breadboard
- IC 7493 (Binary Counter)
- Wires, wire cutter, tweezers

## Theory

The 4-bit binary counter is an IC which counts from 0 to 15, and outputs the result as a 4-bit binary number. It requires a clock signal to operate. At each clock pulse, the counter increments by 1, and the output is updated.

We will use our circuit $M$ (part (b)) to generate the clock signal of frequency 2 Hz, meaning the counter will increment by 1 every 0.5 s.

The output of the counter will be fed to circuit $C$ (part (a)), to display the number on the 7-segment display. In effect, we will see the number on the display counting from 0 to 15 periodically.

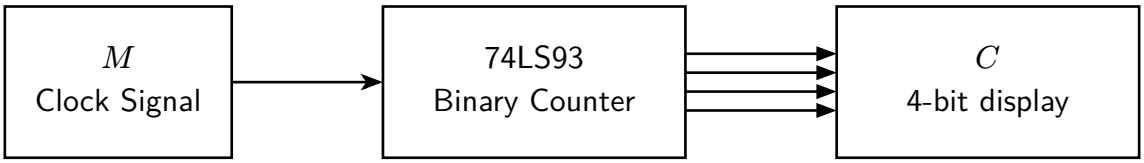



**Figure 6:** Block diagram of the overall circuit

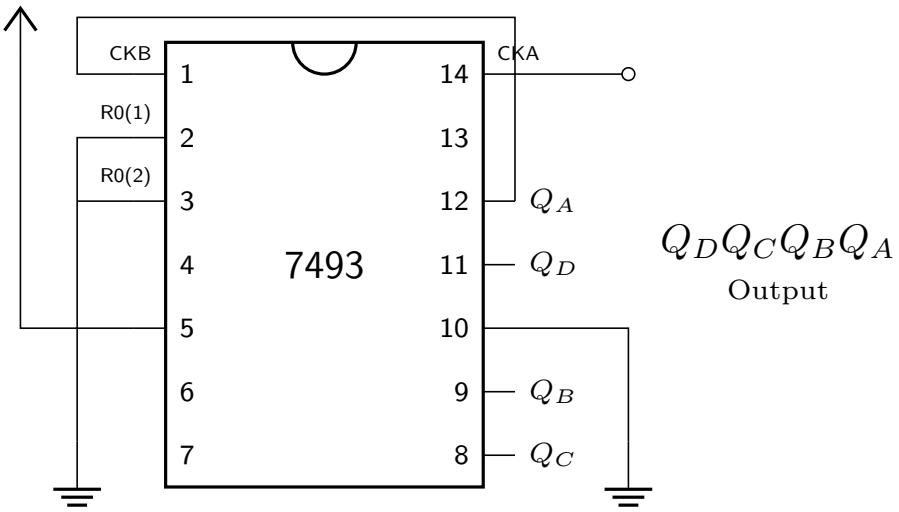



**Figure 7:** Connection diagram of the 4-bit binary counter (IC 7493)

## Procedure

1. Connect the 4-bit binary counter to the breadboard. Make the external connections according to the diagram.
2. Connect the clock signal from $M$ to the binary counter, to the CKA input pin.
3. Connect the output bits of the binary counter to the inputs of circuit $C$.
4. Verify that the circuit correctly displays the numbers in sequence.

## Result

The circuit correctly cycles through the numbers from 0 to 15 in sequence, and displays them on the two 7-segment displays in base 10.